REMARKS

Claims 1-35 are patentable over Jones et al. (5,639,695) in view of Ohsawa et al (6,093,970).

With regards to Jones et al., the Examiner states:

> Jones discloses a semiconductor package with (1) providing **a circuit board strip including a plurality of unit circuit boards**, each unit circuit board having ... (Office Action, pages 2-3, emphasis added.)

The Examiner's statement is respectfully traversed. Jones et al. teaches individual BGA packages and the Examiner has failed to callout where Jones et al. teaches or suggests "a circuit board strip including **a plurality** of unit circuit boards" as asserted by the Examiner. For example, with reference to FIG. 2, Jones et al. teaches:

> FIG. 2 illustrates a cross-sectional view of an embodiment of **a perimeter BGA package** according to the present invention ... (Col. 1, lines 65-67, emphasis added.)

Ohsawa et al. does not cure this deficiency in Jones et al. Specifically, the Examiner cites Ohsawa et al. as teaching:

> ... Ohsawa discloses a semiconductor device with (1) ... **singulating** the circuit board strip into semiconductor packages (see Figure 2G). (Office Action, page 10, emphasis added.)

Thus, the Examiner has failed to callout where Jones et al and Ohsawa et al., either alone or in combination, teach or suggest "a circuit board strip including **a plurality** of unit circuit boards" as asserted by the Examiner.

As set forth in MPEP § 2143.03, at page 2100-133, Rev. 2, May 2004:

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> To establish *prima facie* obviousness of a claimed invention, **all the claim limitations must be taught or suggested** by the prior art. (Emphasis added.)

Further, Applicants respectfully submit that one of skill in the art would have no motivation to combine Jones et al. with Ohsawa et al. as asserted by the Examiner.

Applicants note that Jones et al. teaches:

> Substrate 11 typically is formed from an **organic epoxy-glass resin based material, such as bismaleimide-triazin (BT) resin or FR-4 board**. (Col. 2, lines 15-17, emphasis added.)

Similarly, Jones et al. teaches:

> When substrate 31 and support substrate 32 **comprise an organic epoxy-glass resin**, BGA package 30 has a height 51, which is on the order of 1.0 to 1.5 mm. (Col. 4, lines 36-39, emphasis added.)

In stark contrast, Ohsawa et al. teaches:

> FIGS. 2(A) to (I) are cross-sectional views showing the process steps for making **a film circuit** and **making a reinforcing plate adhere to the back surface of the film circuit** in accordance with the present invention.. (Col. 4, lines 62-65.)

Further, with respect to FIG. 2G, Ohsawa et al. teaches:

> Next, as shown in FIG. 2(G), the coated underlayer 14 and the aluminum layer 13 serving as an etching stopper **are etched out** with the leads 3, . . . , 3 used as a mask. (Col. 6, lines 21-23, emphasis added.)

Applicants respectfully submit the Examiner has failed to callout how the resin based substrate of Jones et al. could be etched using the film circuit etching process of Ohsawa et al. More generally, Applicants respectfully submit that one of skill in the art would have no motivation to modify the resin based substrate process of Jones et al. with the film circuit

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process of Ohsawa et al. as suggested by the Examiner as a resin based substrate is substantially different than a film circuit as those of skill in the art understand.

As set forth in the MPEP 2143.01, at page 2100-131, Rev. 2, May 2004:

> The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. (Emphasis in original.)

Further, Applicants respectfully submit that the Examiner is using improper hindsight reconstruction to deprecate the Applicants' claimed invention.

For at least the above reasons, Jones et al. in view of Ohsawa et al. does not teach or suggest:

> A method for fabricating semiconductor packages, the method comprising:
> **providing a circuit board strip including a plurality of unit circuit boards**, each unit circuit board having a plurality of first ball lands formed at a first major surface thereof, a plurality of bond fingers formed at an opposite second major surface thereof, vias through the circuit board each electrically connected between a bond finger and a first ball land, and a through hole between the first and second major surfaces;
> **receiving in each through hole a semiconductor chip** having a first major surface, and an opposite second major surface provided with a plurality of input/output pads thereon, wherein the second major surface of the chip faces in the same direction as the second major surface of the respective circuit board;
> electrically connecting the input/output pads of each semiconductor chip with associated ones of the bond fingers of the respective circuit board;
> **encapsulating the semiconductor chips, and filling the through hole of each unit circuit board of the circuit board strip using an encapsulating material**;
> fusing conductive balls on the first ball lands of each unit circuit board;
> **singulating the circuit board strip into semiconductor packages respectively corresponding to the unit circuit boards**,

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as recited in Claim 1, emphasis added. Accordingly, Claim 1 is allowable. Claims 2-35, which depend from Claim 1, are allowable for at least the same reasons as Claim 1.

Further, Claim 9 recites:

> The method of claim 4, **wherein the one or more closure members are removed after encapsulating the semiconductor chips**. (Emphasis added.)

With respect to Claim 9, the Examiner asserts:

> Jones discloses a semiconductor package with ... (9) wherein the one or more **closure members are removed** after encapsulating the semiconductor chips (see Figure 2) ... (Office Action, pages 2, 6, emphasis added.)

The Examiner's statement is respectfully traversed. Jones et al. teaches that the "closure members" act as a standoff and thus the Examiner has failed to callout where Jones et al. teaches or suggests "wherein the one or more closure members are removed after encapsulating the semiconductor chips" as asserted by the Examiner. For example, with reference to FIG. 2, Jones et al. teaches:

> When BGA package 30 is mounted to PC board 46, **support substrate 32** is in close proximity to PC board 46 and **acts as standoff**, which limits the collapse of conductive solder balls 26 during the mounting process.... (Col. 4, lines 21-24, emphasis added.)

Applicants submit that removing the support substrate 32 would defeat the intended purpose of the support substrate 32 as a standoff. Accordingly, one of skill in the art would have no motivation to remove the support substrate 32.

As set forth in MPEP § 2143.01, at page 2100-131, Rev. 2, May 2004:

> If proposed modification would render the prior art invention being modified **unsatisfactory for its intended purpose, then there is no suggestion or**

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motivation to make the proposed modification. (Emphasis added.)

For this additional reason, Claim 9 is allowable over Jones et al. in view of Ohsawa et al. Claims 10-11 are additionally allowable for reasons similar to Claim 9.

For similar reasons, the Examiner has failed to callout where Jones et al. in view of Ohsawa et al. teaches or suggests:

> The method of claim 7, **wherein the closure members are removed** after encapsulating the semiconductor chips **by inserting a bar into one or more of the main slots in a direction from the second major surface of the circuit board strip** to the first major surface of the second board strip, thereby detaching an associated one of the closure members from the circuit board strip at one side of the associated closure member,

as recited in Claim 12, emphasis added. For this additional reason, Claim 12 is allowable over Jones et al. in view of Ohsawa et al. Claim 13 is additionally allowable for reasons similar to Claim 12.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

CONCLUSION

Claims 1-35 are pending in the application. For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating

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to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant(s).

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 8, 2005

Attorney for Applicant(s) — September 8, 2005 Date of Signature

Respectfully submitted,

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